

**What is claimed is:**

1           1.    A mixed-mode process introducing a hard mask  
2 layer, comprising the steps of:

3           providing a semiconductor structure;

4           sequentially forming a first conductive layer, a  
5 dielectric layer, and a second conductive layer on the  
6 semiconductor structure;

7           forming a first stacked structure in a portion of the  
8 second conductive layer and the dielectric layer, and  
9 revealing the first conductive layer exposed by the first  
10 stacked structure;

11           conformably depositing a mask layer over the first  
12 conductive layer and covering the first stacked structure  
13 thereon; and

14           patterning the mask layer and the first conductive  
15 layer to simultaneously form a capacitor and a second  
16 stacked structure on the semiconductor structure, wherein  
17 the capacitor comprises the first stacked structure, a  
18 patterned mask layer thereon and a patterned first

19       conductive layer therebelow and the second stacked structure  
20       comprises a patterned first conductive layer and a patterned  
21       mask layer stacked thereabove.

1           2. The process as claimed in claim 1, wherein the  
2       patterned mask layer covers sidewalls of the first stacked  
3       structure.

1           3. The process as claimed in claim 1, wherein the  
2       first conductive layer and the second conductive layer  
3       are polysilicon.

1           4. The process as claimed in claim 1, wherein the  
2       dielectric layer is silicon dioxide, silicon nitride,  
3       silicon oxynitride or a high-K material.

1           5. The process as claimed in claim 4, wherein the  
2       high-K material is  $\text{HfO}_2$ ,  $\text{ZrO}_2$ ,  $\text{TiO}_2$ ,  $\text{Al}_2\text{O}_3$ , or  $\text{Ta}_2\text{O}_5$ .

1           6. The process as claimed in claim 1, wherein the  
2       second stacked structure is a conductive wire device.

1           7. The process as claimed in claim 1, wherein the  
2       mask layer is made of non-resist materials different from  
3       a material of the first conductive layer.

1           8. The process as claimed in claim 7, wherein the  
2           mask layer is silicon nitride, silicon dioxide or silicon  
3           oxynitride.

1           9. The process as claimed in claim 1, further  
2           comprising the step of selectively forming a gate  
3           dielectric layer on a portion of the semiconductor  
4           structure before forming the first conductive layer on  
5           the semiconductor structure.

1           10. The process as claimed in claim 9, further  
2           comprising the step of patterning the gate dielectric  
3           layer formed on the semiconductor structure during  
4           patterning of the mask layer and the first conductive  
5           layer to thereby form a second stacked structure, the  
6           second stacked structure having a patterned first  
7           conductive layer, a patterned mask layer and a patterned  
8           gate dielectric layer stacked on the semiconductor  
9           structure.

10          11. The process as claimed in claim 10, wherein  
11          after the capacitor and the second stacked structure are

12 formed on the semiconductor structure, the method further  
13 comprises steps of:

14 forming source/drain regions in the semiconductor  
15 structure on opposite sides of the second stacked  
16 structure;

17 forming a spacer on sidewalls of the second stacked  
18 structure; and

19 selectively forming a silicide layer on top of the  
20 source/drain regions to form a MOSFET device comprising  
21 the second stacked structure on the semiconductor  
22 structure.

1 12. A mixed-mode process introducing a hard mask  
2 layer, comprising the steps of:

3 providing a semiconductor structure having a  
4 conductive region, a metal-oxide semiconductor (MOS)  
5 region and a capacitor region;

6 sequentially forming a first conductive layer, a  
7 dielectric layer, and a second conductive layer on the  
8 semiconductor structure;

9           forming a first stacked structure in a portion of  
10       the second conductive layer and the dielectric layer  
11       within the capacitor region, and revealing the first  
12       conductive layer exposed by the first stacked structure;

13           conformably depositing a mask layer over the first  
14       conductive layer and covering the first stacked structure  
15       thereon;

16           respectively forming a first pattern, a second  
17       pattern and a third pattern on the mask layer within the  
18       capacitor region, the conductive region and the MOS  
19       region, wherein the first pattern covers the mask layer  
20       over the first stacked structure and wherein the second  
21       pattern and the third pattern respectively covers other  
22       portion of the mask layer; and

23           patterning the mask layer and the first conductive  
24       layer to simultaneously form a capacitor, a second  
25       stacked structure and a third stacked structure on the  
26       semiconductor structure respectively within the capacitor  
27       region, the conductive region and the MOS region, wherein  
28       the capacitor comprises the first stacked structure, a

29 patterned mask layer thereon and a patterned first  
30 conductive layer therebelow and the second stacked  
31 structure and the third stacked structure each comprises  
32 a patterned first conductive layer and a patterned mask  
33 layer thereabove.

1 13. The process as claimed in claim 12, wherein the  
2 patterned mask layer covers sidewalls of the first  
3 stacked structure.

1 14. The process as claimed in claim 12, wherein the  
2 first conductive layer and the second conductive layer  
3 are polysilicon.

1 15. The process as claimed in claim 12, wherein the  
2 dielectric layer is silicon dioxide, silicon nitride,  
3 silicon oxynitride or a high-K material.

1 16. The process as claimed in claim 15, wherein the  
2 high-K material is  $\text{HfO}_2$ ,  $\text{ZrO}_2$ ,  $\text{TiO}_2$ ,  $\text{Al}_2\text{O}_3$ , or  $\text{Ta}_2\text{O}_5$ .

1 17. The process as claimed in claim 12, wherein the  
2 second stacked structure is a conductive wire device.

1           18. The process as claimed in claim 12, wherein the  
2           mask layer is a non-resist material different from a  
3           material of the first conductive layer.

1           19. The process as claimed in claim 18, wherein the  
2           mask layer is silicon nitride, silicon dioxide or silicon  
3           oxynitride.

1           20. The process as claimed in claim 12, further  
2           comprising the step of selectively forming a gate  
3           dielectric layer on a portion of the semiconductor  
4           structure within the MOS region before forming the first  
5           conductive layer on the semiconductor structure.

1           21. The process as claimed in claim 20, further  
2           comprising the step of patterning the gate dielectric  
3           layer formed on the semiconductor structure within the  
4           MOS region during patterning of the mask layer and the  
5           first conductive layer to thereby form a third stacked  
6           structure comprising a patterned first conductive layer,  
7           a patterned mask layer and a patterned gate dielectric  
8           layer stacked on the semiconductor structure.

1           22. The process as claimed in claim 21, wherein  
2           after the capacitor, the second stacked structure and the  
3           third stacked structure are formed on the semiconductor  
4           structure, the method further comprises the steps of:

5                 forming source/drain regions in the semiconductor  
6                 structure on opposite sides of the third stacked  
7                 structure within the MOS region;

8                 forming a spacer on sidewalls of the third stacked  
9                 structure; and

10                selectively forming a silicide layer on top of the  
11                source/drain regions to form a MOSFET device comprising  
12                the third stacked structure on the semiconductor  
13                structure.